CLAIM LISTING

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-35 are canceled

36. (New) A processor chip, comprising:

a Reduced Instruction Set Computer (RISC) core; and

multiple multi-threaded programmable units communicatively coupled with the Reduced Instruction Set Computer core, each of the multiple multi-threaded programmable units comprising a control store and storage for multiple program counters associated with the, respective, multiple threads, each of the multi-threaded programmable units having logic to re-enable availability for execution of a one of multiple threads in response to a signal associated with a memory reference issued by the thread.

37. (New). The processor chip of claim 36,

wherein each of the multiple multi-threaded programmable units comprises a programmable unit having a multi-stage instruction pipeline.

38. (New) A method, comprising:

providing instructions for execution by a processor chip, the processor chip comprising:

a Reduced Instruction Set Computer (RISC) core; and

multiple multi-threaded programmable units, each of the multiple multi-threaded programmable units comprising a control store and storage for multiple program counters associated with the, respective, multiple threads, each of the multi-threaded programmable units having logic to re-enable availability for execution of a

one of multiple threads in response to a signal associated with a memory reference issued by the thread;

wherein at least some of the instructions comprise instructions to handle network protocol data path operations for execution as threads by the multiple multi-threaded programmable units.

39. (New) The method of claim 38, wherein at least some of the instructions comprise instructions to handle network protocol exception packets by the Reduced Instruction Set Computer (RISC) core.

40. (New) A processor chip, comprising:

multiple multi-threaded programmable units, each of the multiple multi-threaded programmable units comprising a control store and storage for multiple program counters associated with the, respective, multiple threads, each of the multi-threaded programmable units having logic to re-enable availability for execution of a one of multiple threads in response to a signal associated with a memory reference issued by the thread.

41. (New). The processor chip of claim 40,

further comprising a Reduced Instruction Set Computer (RISC) core.